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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,725	12/28/2000	James S. Burns	2207/10120	6772

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EXAMINER	
GOLE, AMOL V	

ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 12/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,725	BURNS ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/28/00, 4/3/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

    1. Declaration, and Drawings (4/03/01)

    These papers have been placed of record in the file.

2. Claims 1-18 have been examined.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of the scheduler comprising of a first and second pipeline stage, each in alignment with a processor clock cycle must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. It is the suggested by the examiner to indicate this limitation by splitting the scheduler (fig. 1,105) into two stages and labeling them accordingly.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A METHOD AND APPARATUS FOR MAPPING IN ONE STAGE AND MERGING AND REMAPPING IN A SECOND STAGE A PLURALITY OF INSTRUCTION GROUPS TO A PLURALITY OF FUNCTIONAL UNITS.

Claim Objections

5. Claim 13 objected to because of the following informalities:

6. On pg. 12, line19, the word "be" should be inserted the words "to executed" for the purposes of grammatical correctness.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **1-6 and 13-18** are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata et al (US005430851A).

9. In regard to claim 1:

10. Hirata et al. disclose a processor (col. 4, line 50), comprising,

11. a plurality of pipelined functional units for executing instructions (Fig. 3, elements 16-18);

12. a scheduler (Fig. 3, instruction setup units 14 and instruction schedule unit 15), coupled to the plurality of functional units (fig. 3), programmed for independently mapping instructions, received from at least two separate instruction groups, to at least a portion of the functional units (independent instruction setup units for each instruction stream [col. 5, lines 55-59] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]) during a first stage (fig. 3, instruction setup units 14 comprise of the first stage).

13. wherein the scheduler is programmed to merge (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remap the instructions (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) to at least a portion of the functional units, based on functional unit requirements and availability (signal R, col. 6, lines 54-56), during a second stage (fig. 3, instruction schedule unit 15 comprises of a second stage).

14. In regard to claim 2:

15. Hirata et al. further disclose that the scheduler is programmed to deliver the instruction to the portion of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 3 and col. 8, 51-56).

16. In regard to claim 3:

17. Hirata et al. further disclose that the scheduler, in alignment with the processor clock cycle (col. 7, lines 52-55), is programmed to map the instructions during a first stage of the pipeline (instruction setup unit) for the functional units, and programmed to merge and remap the instructions during a second stage (instruction schedule unit) of the pipeline for the functional units.

18. In regard to claim 4:

19. Hirata et al. further disclose that the functional units execute an increased number of instructions operating at a given clock rate (col. 2, lines 61-64).

20. In regard to claim 5:

21. Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

22. In regard to claim 6:

23. Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

24. In regard to claim 13:

25. Hirata et al. disclose a method of dispersing instructions (instruction schedule unit distributes instructions to the functional units, col. 6, lines11-14) to be executed by a processor (col. 4, line 50), comprising:

26. mapping instructions (instruction setup units [fig. 3, 14] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]), received from at least two separate, independent instruction groups (instruction streams, col. 5, lines 55-59), to at least a portion of a plurality of pipelined functional units during a first stage (instruction setup unit 14);

27. merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping the instructions (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) to at least a portion of functional units, based on functional unit requirements and availability (signal R, col. 6, lines 54-56), during a second stage (instruction schedule unit 15).

28. In regard to claim 14:

29. Hirata et al. further disclose the step of delivering the instructions to portions of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 3 and col. 8, 51-56).

30. In regard to claim 15:

31. Hirata et al. further disclose that the step of merging and remapping includes merging and remapping the instructions to the portion of functional units to allow execution of an increased number of instructions at a given clock rate (co. 2, lines 61-64).

32. In regard to claim 16:

33. Hirata et al. further disclose that the step of mapping includes mapping the instructions, in alignment with a processor clock cycle (col. 3, lines 38-40), during a first stage (instruction setup unit 14) of the pipeline for the functional units, and merging and remapping the instructions, in alignment with the processor clock cycle (col. 7, lines 52-55), during a second stage (instruction schedule unit 15) of the pipeline for the functional units.

34. In regard to claim 17:

35. Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

36. In regard to claim 18:

37. Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

39. Claims **7-12** are rejected under 35 U.S.C. 103(a) for the same reasons as claims 1-6 above as being unpatentable over Hirata et al. (US005430851A) in view of Tannenbaum ("Structured Computer Organization," Prentice-Hall, 1984, pp. 10-12).

40. Hirata et al. differs from the applicant's invention in that it does not teach that instructions on a machine-readable medium comprise instructions for performing the limitations of claims 1-6 of the applicant's invention.

41. However Tannenbaum teaches that any instruction executed by hardware can also be simulated in software (pg 11, para. 4, lines 1-2).

42. One of ordinary skill in the art at the time of the invention would have converted the Hirata et al. reference to software i.e. instructions on a machine readable medium from the teachings of Tannebaum.

43. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the Hirata et al. processor by converting it to instructions on a machine-readable medium.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

AVG

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100